EXPRESS MAIL LABEL NO. EL814475048US



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

: Atty. Docket: POU920010005US1

Marvin J. RICH et al.

: APPLICATIONS BRANCH

Serial No. (not yet assigned)

Filed: Herewith

For: SIZ

SIZE REDUCTION TECHNIQUES FOR VITAL

COMPLIANT VHDL SIMULATION MODELS

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents Washington, D. C. 20231

SIR:

The attached Form PTO-1449 provides a listing of information which may be relevant to the subject application. This IDS is not intended as a representation that better art is not available, nor that the information provided is prior art.

This I	DS is submitted under:
<u>_XX</u>	37 CFR 1.97(b) - No Fee.
	37 CFR 1.97(c) - No Fee, with Certification.
	37 CFR 1.97(c) - Fee.
	27 CED 4 07(d) For Cortification & Potition

The Commissioner is authorized to charge any required fees under 37 CFR 1.17(p) and (i) (1) to Deposit Account No. **09-0463**.

Date: 1/0×/0×

Respectfully submitted,

/ Jose Gutman

Registration No. 35,171

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Form PTO-1449 U.S. Dept. of Commerce Patent & Trademark Office				Atty. Docket: POU920010005US1 Serial No. (not yet assigned)							
		of Documents	S	Applicant: Marvin J. RICH et al.							
Cited by Applicant (Use several sheets if necessary)				Filing D	Filing Date: Herewith Group: (not y			et assigned)			
U.S. PATENT DOCUMENTS											
Ex'rs In'i		Document Number	Date	· · · · · · · · · · · · · · · · · · ·	Name	Class	Sub- class	Filing Date, if applicable			
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conformance and not considered. Include copy of this form with next communication to applicant.